
REMARKS

This responds to the Office Action mailed on September 9, 2004.

Claims 1, 5, 6, 13, 15, 20, 22, 24, 28, 39, 79, and 82 are amended. Claims 1-49, and 74-84 remain pending in this application.

Independent claims 1, 6, 13, 22, 79, and 82 are amended for clarity.

Dependent claims 5, 15, 20, 24, 28, and 39 are amended only to rewrite these claims in independent form. These claims are not amended because of a rejection. The amendments do not narrow the scope of these claims.

Claim Objection

Claim 79 was objected to due to informalities. Claims 79 and 82 have been amended to correct the word order error indicated in the Office Action.

§102 Rejection of the Claims

Claims 1-4, 6-14, 16-19, 22, 23, 25-27, 30-38, and 74-84 were rejected under 35 USC § 102(b) as being anticipated by Hassoun et al. (U.S. 6,587,534).

Claim 1 is amended for clarity. As amended, claim 1 recites, among other things, "a command react circuit connected to the selector for enabling the selector to select the second delayed signal based on a first state of a command signal, while the external and internal clock signals are synchronized, to provide the internal clock signal and for enabling the selector to select the first delayed signal based on a second state of the command to provide the internal clock signal". Applicant is unable to find in Hassoun "a command react circuit connected to the selector for enabling the selector to select the second delayed signal based on a first state of a command signal, while the external and internal clock signals are synchronized, to provide the internal clock signal and for enabling the selector to select the first delayed signal based on a second state of the command to provide the internal clock signal". Accordingly, Applicant requests that the rejection of claim 1 be reconsidered and withdrawn and that claim 1 and dependent claims 2-4 be allowed.

Claim 6 is amended for clarity. As amended, claim 6 recites, among other things, "a command react circuit connected to the selector for enabling the selector to select the second

delayed signal based on a first state of a command signal, while the external and internal clock signals are synchronized, to provide the internal clock signal and for enabling the selector to select the first delayed signal based on a second state of the command to provide the internal clock signal". Applicant is unable to find in Hassoun "a command react circuit connected to the selector for enabling the selector to select the second delayed signal based on a first state of a command signal, while the external and internal clock signals are synchronized, to provide the internal clock signal and for enabling the selector to select the first delayed signal based on a second state of the command to provide the internal clock signal". Accordingly, Applicant requests that the rejection of claim 6 be reconsidered and withdrawn and that claim 6 and dependent claims 7-12 be allowed.

Claim 13 is amended for clarity. As amended, claim 13 recites, among other things, "a command react circuit connected to the selector, the command react circuit including a first input for receiving a command signal, a second input for receiving a phase detect signal, and an output node responsive to the command and phase detect signals for providing a command set signal to enable the selector to provide the internal clock signal based on the second delayed signal when the command signal is activated while the external and internal clock signals are synchronized, and to provide the internal clock signal based on the first delayed signal when the command signal is deactivated". Applicant is unable to find in Hassoun "a command react circuit connected to the selector, the command react circuit including a first input for receiving a command signal, a second input for receiving a phase detect signal, and an output node responsive to the command and phase detect signals for providing a command set signal to enable the selector to provide the internal clock signal based on the second delayed signal when the command signal is activated while the external and internal clock signals are synchronized, and to provide the internal clock signal based on the first delayed signal when the command signal is deactivated". Accordingly, Applicant requests that the rejection of claim 13 be reconsidered and withdrawn and that claim 13 and dependent claims 14, and 16-19 be allowed.

Claim 22 is amended for clarity. As amended, claim 22 recites, among other things, "a command react circuit connected to the selector, the command react circuit including a first input for receiving a command signal, a second input for receiving a phase detect signal, and an output node responsive to the command and phase detect signals for providing a command set signal to

enable the selector to provide the internal clock signal based on the second delayed signal when the command signal is activated while the external and internal clock signals are synchronized, and to provide the internal clock signal based on the first delayed signal when the command signal is deactivated". Applicant is unable to find in Hassoun "a command react circuit connected to the selector, the command react circuit including a first input for receiving a command signal, a second input for receiving a phase detect signal, and an output node responsive to the command and phase detect signals for providing a command set signal to enable the selector to provide the internal clock signal based on the second delayed signal when the command signal is activated while the external and internal clock signals are synchronized, and to provide the internal clock signal based on the first delayed signal when the command signal is deactivated". Accordingly, Applicant requests that the rejection of claim 22 be reconsidered and withdrawn and that claim 22 and dependent claims 23, and 25-27 be allowed.

Claim 30 recites, among other things, "a command react circuit connected to the selector, the command react circuit including a first input for receiving a command signal, a second input for receiving a phase detect signal, and an output node responsive to the command and phase detect signals for providing a command set signal to enable the selector to replace the first delayed signal with the second delayed signal when the command signal is activated while the external and internal clock signals are synchronized and to enable the selector to replace the second delayed signal with the first delayed signal when the command signal is deactivated". Applicant is unable to find in Hassoun "a command react circuit connected to the selector, the command react circuit including a first input for receiving a command signal, a second input for receiving a phase detect signal, and an output node responsive to the command and phase detect signals for providing a command set signal to enable the selector to replace the first delayed signal with the second delayed signal when the command signal is activated while the external and internal clock signals are synchronized and to enable the selector to replace the second delayed signal with the first delayed signal when the command signal is deactivated". Accordingly, Applicant requests that the rejection of claim 30 be reconsidered and withdrawn and that claim 30 and dependent claims 31-38 be allowed.

Claim 74 recites, among other things, "selecting a second delayed signal among the multiple delayed signals to generate the internal clock signal when a command signal is activated

while the external and internal clock signals are synchronized' and "reselecting the first delayed signal to generate the internal clock signal when the command signal is deactivated". Applicant is unable to find in Hassoun "selecting a second delayed signal among the multiple delayed signals to generate the internal clock signal when a command signal is activated while the external and internal clock signals are synchronized' and "reselecting the first delayed signal to generate the internal clock signal when the command signal is deactivated". Accordingly, Applicant requests that the rejection of claim 74 be reconsidered and withdrawn and that claim 74 and dependent claims 75-78 be allowed.

Claim 79 recites, among other things, "reducing the amount of delay by a delay quantity when a command signal is activated while the external and internal clock signals are synchronized" and "before the external and internal clock signals are detected as out of synchronism". Applicant is unable to find in Hassoun "reducing the amount of delay by a delay quantity when a command signal is activated while the external and internal clock signals are synchronized" and "before the external and internal clock signals are detected as out of synchronism". Accordingly, Applicant requests that the rejection of claim 79 be reconsidered and withdrawn and that claim 79 and dependent claims 80 and 81 be allowed.

Claim 82 recites, among other things, "increasing the amount of delay by a delay quantity when a command signal is activated while the external and internal clock signals are synchronized" and "before the external and internal clock signals are detected as out of synchronism". Applicant is unable to find in Hassoun "increasing the amount of delay by a delay quantity when a command signal is activated while the external and internal clock signals are synchronized" and "before the external and internal clock signals are detected as out of synchronism". Accordingly, Applicant requests that the rejection of claim 82 be reconsidered and withdrawn and that claim 82 and dependent claims 83 and 84 be allowed.

Allowable Subject Matter

Claims 5, 15, 20, 21, 24, 28, 29, 39, and 40 were objected to as being dependent upon a rejected base claim, but were indicated to be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 5, 15, 20, 24, 28, and 39 are rewritten in independent form. Claim 29 depends from claim 28. Claim 40 depends from claim 39. Thus, all of the claims 5, 15, 20, 21, 24, 28, 29, 39, and 40 are now in condition for allowance.

Applicant acknowledges the allowance of claims 41-49.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's representative (612) 373-6969 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,


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By his Representatives,

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Date October 29, 2004

By


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